DESCRIPTOR-BASED LOAD BALANCING

Koray Oner
Jeremy Dion

ABSTRACT OF THE DISCLOSURE

[0130] A multiprocessor switching device substantially implemented on a single CMOS integrated circuit is described in connection with a descriptor-based packet processing mechanism for use in efficiently assigning and processing packets to a plurality of processors. A plurality of descriptors associated with each packet transfer are written back to memory in order, divided into subset groups and assigned to processors, where each processor searches the assigned subset for EOP and associated SOP descriptors to process.